Electronic Version
Stylesheet Version v1.1.1

Description

[DIGITAL TO ANALOG CONVERTER USING TUNNELING CURRENT ELEMENT]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The invention generally relates to electrical circuit design, and more particularly to a digital-to-analog converter using tunneling current characteristics of a field effect transistor (FET) ultra-thin gate oxide.

[0003] Description of the Related Art

[0004] Analog-to-digital converters convert analog signals such as speech, music, and video and transform it into a digital form, which can be more readily processed by most conventional computers and microprocessors. A typical analog-to-digital converter is the parallel encoder, which utilizes a bank of voltage comparators and a bank of resistors to simultaneously compare an analog input signal to a set of reference voltages.

[0005] These devices usually comprise a stable reference voltage and a series of equal resistors, which form a voltage-dividing sequence between the reference voltage and ground. For example, for a 3-bit converter, 2^x = number of resistors used, where x = 3 for a 3-bit converter, thus 2^3 = 8 resistors are used. These devices further include a set of voltage comparators, which for the 3-bit converter example would require 2^3 1 = 7 comparators. Also, these devices include an encoder circuit, which reads the comparator outputs (high or low voltage), and produces a 2-bit binary output for each comparator.

[0006] Similarly, digital-to-analog converters take a binary input and convert it into an analog form using a stable reference voltage, a connection of resistors referred to as a ladder (for example, an R-2R ladder), a series of FET switches, and operational amplifier output circuitry.

[0007] Conventionally, digital-to-analog converters use banks of large resistors to make voltage dividers for each bit of a digital input. The resistors have higher than desired tolerance and require large areas for layout as well as power consumption. Moreover, the conventional digital-to-analog converters are subject to several errors including saturation errors, resolution and quantization errors,

and conversion errors.

[0008] Therefore, due to the limitations of the conventional devices, there is a need for a novel digital-to-analog converter, which provides an accurate voltage divider and overcomes the drawbacks of the conventional devices.

SUMMARY OF INVENTION

[0009] The invention provides a digital-to-analog converter comprising a voltage source supply; a voltage division stack (voltage divider) connected to the voltage source supply; a multiplexer connected to the voltage division stack; a digital circuit (decoder), such as a digital decoder or a NAND device, connected to the multiplexer; an analog circuit, such as an operational amplifier, connected to the multiplexer; and an input binary word source connected to the digital circuit; wherein outputs of the digital circuit are input into the analog circuit and converted as analog output. According to the invention, the multiplexer comprises any of a n-type field effect transistor (NFET), a p-type field effect transistor (PFET), and a combination thereof. The digital-to-analog converter further comprises a capacitor connected to the analog circuit and a binary-weighted tunneling current device connected to the digital circuit. Moreover, the multiplexer and the ca-

pacitor comprise an oxide of at least 5 nm in thickness. Furthermore, the tunneling current device outputs tunneling current, wherein the tunneling current is adjusted in proportion to a binary weight of the input binary word source. In another embodiment, the digital-to-analog converter further comprises a node coupled to the digital circuit; at least one current supply FET coupled to the node; and an output FET operable for supplying a current proportional to a current of the current supply FET, wherein the current supply FET is operable for maintaining voltage on the node constant. Additionally, the voltage division stack comprises an NFET transistor in parallel with a tunneling NFET.

[0010] Another embodiment of the invention provides a method of converting a digital signal into an analog signal, wherein the method comprises arranging a plurality of NFETs into a voltage division stack; applying a regulated output of voltage to the voltage division stack;applying a binary-weighted input word to a digital circuit; applying a voltage output of the voltage division stack to each of a multiplexer and the digital circuit; generating a digital output from the multiplexer and the digital circuit; inputting the digital output into an analog circuit; andcon-

verting the digital output into an analog output. The method further comprises connecting a binary-weighted tunneling current device to the digital circuit, wherein the tunneling current device outputs tunneling current, wherein the tunneling current is adjusted in proportion to a binary weight of the input binary word source, and wherein the voltage division stack comprises an NFET transistor in parallel with a tunneling NFET.

[0011] The invention provides a single stack of NFETs properly biased to provide an accurate voltage divider. This tunneling voltage divider is smaller and lower in power than traditional resistor stack voltage references and allows a smaller and lower power digital-to-analog converter to be designed.

[0012] Some advantages of this invention are achieved by using small area NFETs in a division stack, instead of using conventional resistors. The minimum required area of the NFETs is determined such that mismatches in threshold voltage and gate tunneling current characteristics between the NFETs are minimized to very low values. The stack of NFETs of ultra-thin gate oxide operates in a gate current tunneling mode and performs the function of voltage division. A significant characteristic of the gate tunneling cur-

rent is that with all the NFETs having the same area, the same current flows through the FETs when the voltage drop across each gate oxide element is the same. Since the gate tunneling current is proportional to the area of the oxide, power dissipation is kept to a minimum by minimizing the area of each NFET.

[0013] These, and other aspects of the invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the invention without departing from the spirit thereof, and the invention includes all such modifications.

BRIEF DESCRIPTION OF DRAWINGS

[0014] The invention will be better understood from the following detailed description with reference to the drawings, in which:

[0015] Figure 1 is a graphical representation illustrating the tunneling current characteristics as a function of oxide thick-

ness for different values of gate voltage according to an embodiment of the invention;

[0016] Figure 2 is a schematic diagram illustrating the voltage divisions according to an embodiment of the invention;

[0017] Figure 3 is a graphical representation illustrating the sigma of threshold voltage mismatch versus NFET device area according to an embodiment of the invention;

[0018] Figure 4 is a graphical representation illustrating the change in threshold voltage versus substrate doping according to an embodiment of the invention;

[0019] Figure 5 is a graphical representation illustrating the gate current versus the gate voltage according to an embodiment of the invention;

[0020] Figure 6 is a schematic diagram illustrating a voltage division stack according to an embodiment of the invention;

[0021] Figure 7 is a circuit diagram of a digital-to-analog converter according to an embodiment of the invention;

[0022] Figure 8 is a circuit diagram of a digital-to-analog converter using tunneling current according to an embodiment of the invention; and

[0023] Figure 9 is a flow diagram illustrating a preferred method of an embodiment of the invention.

DETAILED DESCRIPTION

[0024] The invention and the various features and advantageous details thereof are explained more fully with reference to the non-limiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[0025] As previously mentioned, there is a need for a digital-to-analog converter, which provides an accurate voltage divider and overcomes the drawbacks of the conventional devices. Referring now to the drawings, and more particularly to Figures 1 through 9, there are shown preferred embodiments of the invention.

[0026] Figure 1 shows the tunneling current characteristics as a function of oxide thickness for different values of gate voltage. The oxide thickness is defined by an electrical

equivalent thickness measurement in the inversion mode. As shown in the graph, as the oxide thickness increases, the gate current decreases for various values of gate voltage (for example, for gate voltages of 0.2 V, 0.4 V, 0.6 V, 0.8 V, and 1.0 V). The characteristics of the gate tunneling current for ultra-thin gate oxides is an essential element that allows voltage division between serially connected FETs in the configuration of a voltage division stack as shown in Figures 2 and 6. For FETs with the same gate oxide thickness and equal oxide areas, the gate tunneling currents of the FETs are equal when the voltages applied across the gate oxides are equal. Figure 2 shows the basic configuration of an embodiment of the invention to create voltage divisions to any degrees as desired. The case shown in Figure 2 is for a stack of n NFETs all of equal oxide area A, biased in inversion, and connected to a power source of V_{DD}. The different voltage levels generated by the stack are: $[(n-1) \times V_{DD}/n]$, $[(n-2) \times V_{DD}/n]$, $[(n-3) \times V_{DD}/n]$, $[(n-4) \times V_{DD}/n]$, $[(n-5) \times V_{DD}/n]$, $[(n-6) \times V_{DD}/n]$, $[(n-7) \times V_{DD}/n]$, $[(n-8) \times V_{DD}/n]$...$[4 \times V_{DD}/n]$, $[3 \times V_{DD}/n]$, $[2 \times V_{DD}/n]$, and $[V_{DD}/n]$. The configuration shown in Figure 2 is intended to demonstrate how the stack of n NFETs could be used to generate several voltage levels

depending on the value of n. As such, the invention provides a novel use of tunneling FET elements arranged as a division stack, as provided in Figures 2 and 6, in designing a digital-to-analog converter.

[0027] The NFETs are made of zero threshold voltage devices, which allow the NFET to be in inversion even at very small gate voltages so that the gate tunneling current is repeatable and predictable based only on the oxide thickness. According to the invention, oxide thickness variations between the devices with close proximity on the same chip are better than 1%. Moreover, the voltage division changes due to temperature variations are less than 3%.

[0028] The length and width, and hence the area of each FET in the division stack is designed to minimize variations in the gate current due to threshold voltage tolerance and mismatches between the FETs. The appropriate minimum area of the devices is determined as follows for a typical case (as an example) of 1.2 nm physical oxide thickness. Figure 3 shows the sigma of threshold voltage mismatch between the FETs as a function of the device area. As the device area (length and width) increases, the threshold voltage tolerance and mismatches decreases. This is important in determining a minimum area requirement for

the FETs. It should be noted from Figure 3, that as the area of the FET decreases, the mismatch in the threshold voltage between FETs increases. The threshold voltage of the FET could have an effect on the gate tunneling current in inversion. Thus, it is valuable to determine a minimum area requirement so that the mismatches between the threshold voltages of the FETs, and hence differences in their gate tunneling current characteristics, be negligibly small. From Figure 3, at a device area of 4 μm^2 the (3xSigma) variations in threshold voltage are less than 10 mV.

[0029] Figure 4 shows the change in threshold voltage due to changes in silicon substrate surface doping, where the reference point (no change in Vt) is defined at a doping of 5E15 $/cm^3$. From this result, a change of + / - 10 mV in threshold voltage is produced by a change in surface doping from 5E15 to 6.876E15 $/cm^3$ and 3.668E15 $/cm^3$, respectively. Applying this result to the corresponding changes in gate current of the FET, the results are shown in Figure 5. The results indicate that with a device area of 4μm^2, the changes and mismatches in threshold voltage between the FETs will result in changes in gate current well below 1%. Thus, the length and width of the FETs are

all designed to 2 μm x 2 μm; i.e. an area of 4 μm^2. This is significant because it is highly desirable to keep the FET device area in the division stack as small as possible, but at the same time minimize threshold voltage mismatches and in turn minimize differences in gate tunneling current characteristics of the FETs. Thus, it is desirable to determine minimum area requirement for the FETs.

[0030] The preferred embodiment includes having a band gap reference voltage source for the supply V_{DD} connected to the FET division stack. This will ensure reduction of voltage supply tolerance and variations and will minimize the effect on the voltage division stack.

[0031] Another feature of the invention is an additional control to cut off (bypass) any combination of the FETs in the voltage division stack. As shown in Figure 6, this is accomplished by having an NFET transistor in parallel with each tunneling NFET, whereby control signals C_1, C_2, C_3, C_4,...,C_{n-1}, and C_n are applied to the gates of the control transistors. When a control gate, for example, C_n, is low, the control transistor with that control gate is OFF, and the tunneling NFET in parallel with it is active in the voltage division stack. When the control gate C_n is high, the control transistor if ON and the associated tunneling NFET is cut-off

(bypassed) from the voltage division stack. This control allows for changing the voltage division ratios available for digital-to-analog conversion. The control transistors are made of thick oxide (preferably 5 nm or greater gate oxide thickness) instead of ultra-thin gate oxides, such as in conventional devices. This will minimize gate tunneling currents for the control transistors, which may otherwise interfere with the operation of the tunneling NFETs.

[0032] According to an embodiment of the invention, a digital-to-analog converter using tunneling amplifiers is shown in Figure 7. The system comprises a band gap voltage regulator 10 with input as power supply V_D and a regulated output as V_{DD} which is applied to the NFET voltage division stack 15, which is further described in Figures 2 and 6. The outputs of the voltage division stack (n+1) are applied to a multiplexer (MUX) 20 and a [Ln(n+1) / Ln(2)] input word 25 are applied to a digital decoder 30 and the (n+1) outputs are applied to NAND devices 35 which, through control transistors (not shown), feed the (n+1) outputs of the voltage divider stack 15 to an operational amplifier (op amp) 40 with a capacitor 45 connected to its first input and with a DC Offset supply 50 connected to the second input of the operational amplifier 40. The out-

put of the operational amplifier is in analog mode.

[0033] An embodiment using tunneling current to make a fully operable digital-to-analog converter is shown in Figure 8, whereby a voltage reference is compared to the RAIL node which is being fed by a PFET (P1) device. P1 PFET device is controlled by a unity gain op-amp to provide enough current to supply adequate tunneling current to make the RAIL voltage equal to V_{REF}. Digital switch devices and binary-weighted tunneling devices are connected to the RAIL node. The tunneling current is increased or decreased in proportion to the weight of the input binary word (A_0-A_n). The current through the first PFET (P1) is mirrored to a second PFET (P2) and is directed to node V_{out}. Analog output can be in current form or by the addition of the resistor, wherein a voltage output is available. Experimentally, results are highly linear and the current consumption in the tunneling D-A conversion is less than 400na.

[0034] Figure 8 illustrates an alternate embodiment of a digital-to-analog converter using tunneling devices TD1-TD4. Digital inputs A1-A4 are converted to an analog output signal VOUT. A reference voltage of approximately half of the power supply voltage is applied to the VREF input.

This voltage is compared to the voltage on the RAIL node by the OP-AMP. A control voltage CTRL is generated by the OP-AMP which will allow sufficient conduction through PFET P1 to make node voltage RAIL essentially equal to voltage VREF by means of negative feedback. Control voltage CTRL is filtered by decoupling capacitor C1 and is connected to the gate of mirror device P2 which conducts a proportional current into resistor R1.

[0035] The current through P1 is modulated in predictable and linear increments by the digital states of control inputs A1-A4. Switch devices N1-N4 are made large enough such that they function as digital switches and allow gating of current through their respective tunneling devices TD1-TD4 to ground. With the voltage on node RAIL held constant by the OP-AMP, the current through P1, and hence, P2 can be modulated in binary increments by designing the tunneling devices TD1-TD4 to have tunneling currents which increase by binary weighting. This is most easily done by designing their thin-oxide areas "A"to increase by binary weighting. An analog output voltage VOUT is developed across resistor R1 in response to the current through P2. If an analog current output is desired, resistor R1 could be omitted.

[0036] In other words, the circuit shown in Figure 8 draws current from a regulated node and then mirrors this current by multiple amounts as analog output. The currents are drawn by a group of tunneling devices TD1-TD4 that are binary increments.

[0037] According to the flow diagram in Figure 9, an embodiment of the invention provides a method of converting a digital signal into an analog signal is illustrated, wherein the method comprises arranging 101 a plurality of NFETs into a voltage division stack; applying 103 a regulated output of voltage to the voltage division stack; applying 105 a binary-weighted input word to a digital circuit; applying 107 a voltage output of the voltage division stack to each of a multiplexer and the digital circuit; generating 109 a digital output from the multiplexer and the digital circuit; inputting 111 the digital output into an analog circuit; and converting 113 the digital output into an analog output. The method further comprises connecting 115 a binary-weighted tunneling current device to the digital circuit, wherein the tunneling current device outputs tunneling current, wherein the tunneling current is adjusted in proportion to a binary weight of the input binary word source, and wherein the voltage division stack comprises

an NFET transistor in parallel with a tunneling NFET. As mentioned, the multiplexer comprises any of an NFET, a PFET, and a combination thereof. Moreover, the multiplexer and the capacitor comprise an oxide of at least 5 nm in thickness.

[0038] According to the invention, a highly linear low current digital-to-analog converter is provided with very small devices as compared to conventional converters using resistors. Generally, the invention provides a circuit which uses smaller tunneling capacitor structures that are used to provide the required voltage references with better tolerance, and better temperature coefficients. As such, the invention provides a single stack of NFETs properly biased to provide an accurate voltage divider. This tunneling voltage divider is smaller and lower in power than traditional resistor stack voltage references and allows a smaller and lower power digital-to-analog converter to be designed.

[0039] Some advantages of the invention are achieved by using small area NFETs in a division stack, instead of using conventional resistors. The minimum required area of the NFETs is determined such that mismatches in threshold voltage and gate tunneling current characteristics between

the NFETs are minimized to very low values. The stack of NFETs of ultra-thin gate oxide operates in a gate current tunneling mode and performs the function of voltage division. A significant characteristic of the gate tunneling current is that, with all the NFETs having the same area, the same current flows through the FETs when the voltage drop across each gate oxide element is the same. Since the gate tunneling current is proportional to the area of the oxide, power dissipation is kept to a minimum by minimizing the area of each NFET.

[0040] The foregoing description of the specific embodiments will so fully reveal the general nature of the invention that others can, by applying current knowledge, readily modify and/or adapt for various applications such specific embodiments without departing from the generic concept, and, therefore, such adaptations and modifications should and are intended to be comprehended within the meaning and range of equivalents of the disclosed embodiments. It is to be understood that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Therefore, while the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be prac-

ticed with modification within the spirit and scope of the appended claims.